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Design and Simulation of Aerospace Electric Thrusters Using FPGA

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Abstract: This paper addresses the digitization of aerospace electric thruster design to reduce cycle time, cost, and workload. Using the MIL-STD-1553B bus for reliable communication and FPGA as the core processing unit, a simulation model is developed. The system's functionality and stability are verified through waveform analysis and parameter optimization. Results confirm the effectiveness of the FPGA-based control system for continuous and stable operation in thruster digital design.

Keywords: Field Programmable Gate Array (FPGA); MIL-STD-1553B bus; Table lookup method; Pipelining technique.

1. Introduction

In today's era of blowout development of aerospace electric thrusters, in order to solve the problems of long cycle, high cost and heavy workload in the design of traditional thrusters, the design and manufacturing of thrusters are gradually intellectualized and digitized [1]. In order to ensure the quality of digital design and manufacturing of thrusters, modeling and simulation of thrusters are needed, which is one of the important means to ensure quality [2]. When designing digital model of electric thruster, in order to approximate the electronic and mechanical properties of real electric thruster, the real situation of electric thruster should be taken into account, including the communication mode of electric thruster. The MIL-STD-1553B bus with deterministic and reliable transmission is a common mode of communication in aerospace field. In order to save the development time, the packaged MIL-STD-1553B module board card was selected when building the simulation model, and the board card was controlled by the core processing unit.

Field Programmable Gate Array (FPGA), as the core processing unit, can collect and process data in real time and in parallel [3]. In addition, it makes the design simpler and faster, so it is widely used in aerospace, medical, industrial control and other fields [4].

2. System Design Scheme

FPGA chip contains rich logic resources such as pin resources and storage resources, so it can process data quickly and in parallel. The FPGAboard drives the 1553B module of the model of Beijing StD- 1553B Technology Co., LTD through SPI interface. The 1553B module board transmits data to the CAV-1153B-USB simulator through MIL-STD-1553B bus. The final simulator sends the data to the upper computer software by USB for display and storage. The block diagram of the system design scheme is shown in Figure 1.

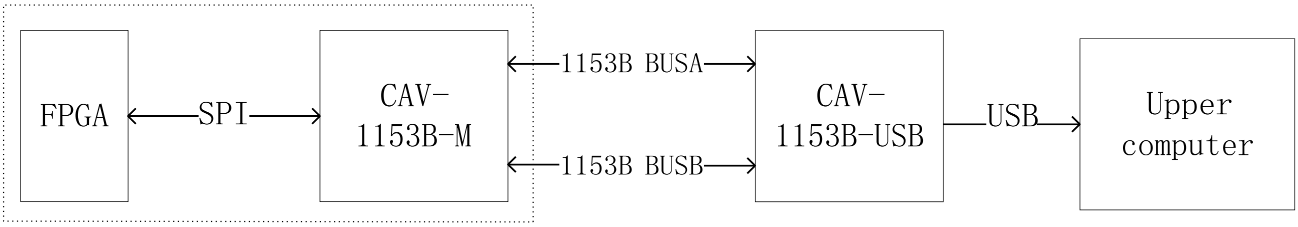

Fig. 1 Block diagram of system structure

In Figure 1, FPGA is the MZ7030FA board, and 1153B boards are CAV-1553B-M-DB boards equipped with CAV-1553B-M. The main interfaces of the boards are shown in Table 1. 1153B emulator is shown in Figure 2.

The left side of the simulator in Figure 2 is the MIL-STD-1553B bus and the right side is the USB interface.

Fig. 2 1153B Simulator

Table 1. Main interface of 1553B board

Interface name	Function	Interface name	Function
SPI_SCK	SPI interface clock	BUSA+	1153B A bus positive signal
SPI_SI	SPI interface data input	BUSA-	1153B A bus negative signal
SPI_SO	SPI interface data output	BUSB+	1153B B bus positive signal
SPI_CE#	SPI interface slice select input	BUSB-	1153B B bus negative signal
INT#	Interrupt request output	GND	Ground signal

3. FPGA Circuit Design and Workflow

3.1. FPGA internal circuit design

FPGA internal logic circuit block diagram is shown in Figure 3.

The external interface of the chip is a SPI-Master interface that drives the 1153B board. Through this interface, the 1153B board is configured and data transmitted. The upper computer instruction from 1153B board card is integrated through the data conversion module and converted in the three states of the state machine. The task state scheduling of 1553B initialization, 1553B idle and 1553B shutdown has been realized. The initial ROM module provides configuration parameters for the initialization of 1153B module, making the 1553B board work in RT, BC, or BM mode. 1553B initialization module the initialization of the 1553B board is completed, and the opening and closing of channels are completed in the module. The sending RAM module stores the data to be sent for reading by the data conversion module. The receiving RAM is used to store data from the 1553B board for subsequent data processing.

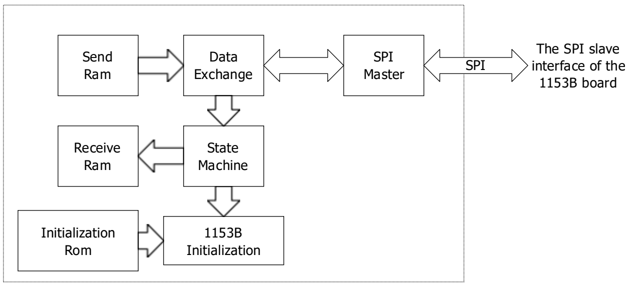

Fig. 3 Block diagram of FPGA internal circuit structure

3.2. Work flow of chip circuit system

The FPGA chip first checks whether the reset time is sufficient. If the time is sufficient, the 1153B card is initialized. Otherwise, the 1153B card is not ready. After the initialization project is complete, check whether a configuration error signal occurs during the initialization. If yes, 1553B fails to be initialized, troubleshoot the cause, and re-initialize the 1153B card. Otherwise, the 1553B board enters the idle state and is ready to receive or send data. In this state, the instructions issued by the 1153B board are parsed and the related command operations are executed. If the parsed instructions are not defined, the 1153B board remains idle. The working flow chart of the system is shown in Figure 4.

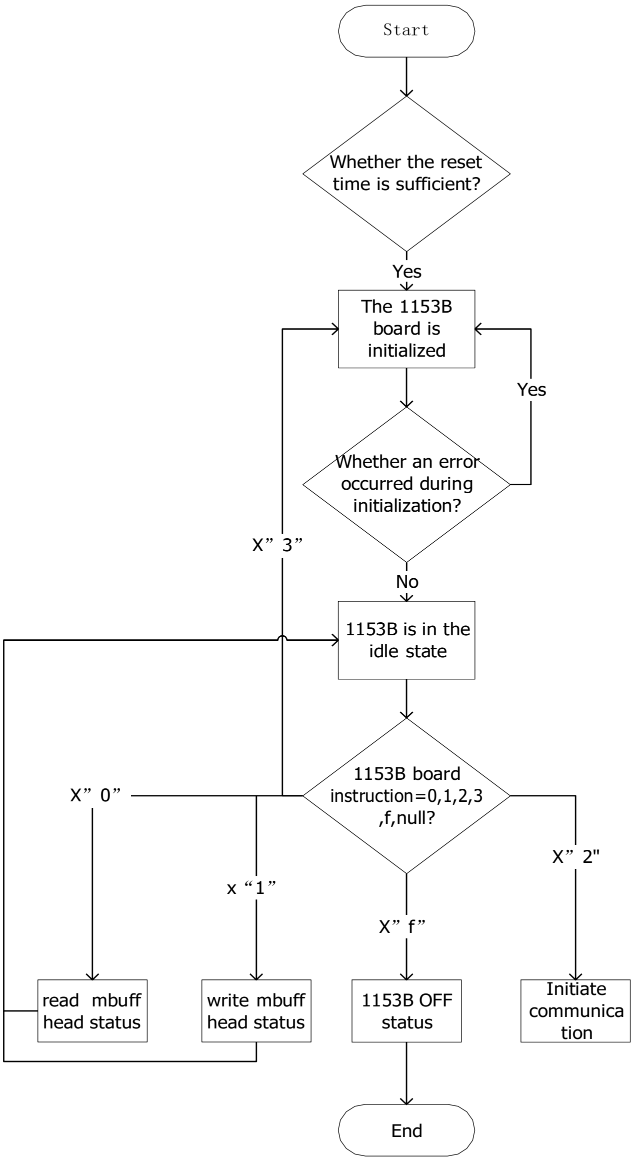
Start
Whether the reset time is sufficient?
Yes
The 1153B board is initialized
Yes
Whether an error occurred during initialization?
X” 3”
No
1153B is in the idle state
1153B board instruction=0,1,2,3 ,f,null?
X” 0”
x “1”
X” f”
X” 2"
read mbuff head status
write mbuff head status
1153B OFF status
Initiate communica tion
End

Fig.4 System flow chart

The initialization process for the 1553B card is as follows: First, the 1153B card is initialized to RT mode. Check whether the 1153B card is successfully configured to RT mode. If the initialization fails, stop the initialization operation. Then configure the sub-address memory required for RT mode communication. The initialization flowchart is shown in Figure 5.

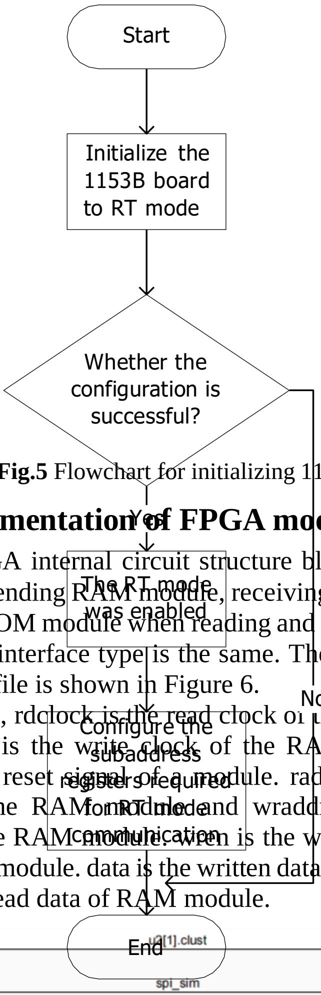
Start
Initialize the 1153B board to RT mode
Whether the configuration is successful?
Yes
No
The RT mode was enabled
Configure the subaddress registers required for RT mode communication
End

Fig.5 Flowchart for initializing 1153B

3.3. Implementation of FPGA module

In the FPGA internal circuit structure block diagram, the structure of sending RAM module, receiving RAM block and initializing ROM module when reading and storing data is the same, so the interface type is the same. The compiled RAM module metafile is shown in Figure 6.

In Figure 6, rdclock is the read clock of the RAM module, and wrclock is the write clock of the RAM module. reset indicates the reset signal of a module. radderss is the read address of the RAM module and wraddress is the write address of the RAM module. wren is the write enable signal for the RAM module. data is the written data of RAM module, and q is the read data of RAM module.

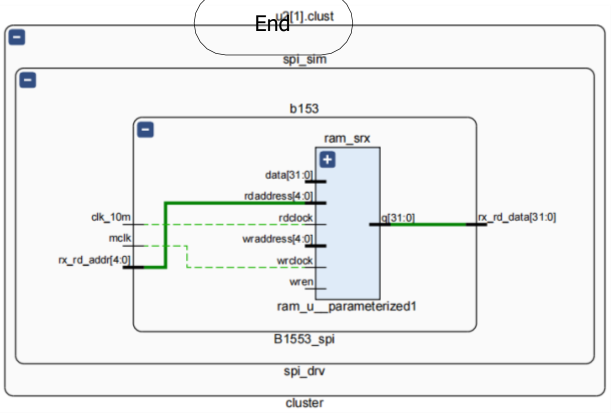

Fig. 6 Meta file diagram of RAM module

Figure 7 is the metafile of spi_master module, in which pclk_i and sclk_i are the tandem clock signal of SPI communication module, rst_i is the reset signal of SPI communication module, and spi_miso_i is the serial data input signal of SPI communication module. spi_mosi_o refers to the serial output data of SPI communication module, spi_sck_o refers to the SPI clock signal of SPI communication module when SPI communication module communicates with 1553B board, spi_ssel_o refers to the slice selection output signal of SPI communication module, wren_i refers to the enable signal of data writing to SPI communication module. wr_ack_o indicates the response signal that data is successfully written to the SPI communication module. Other interfaces are required for debugging and are not introduced.

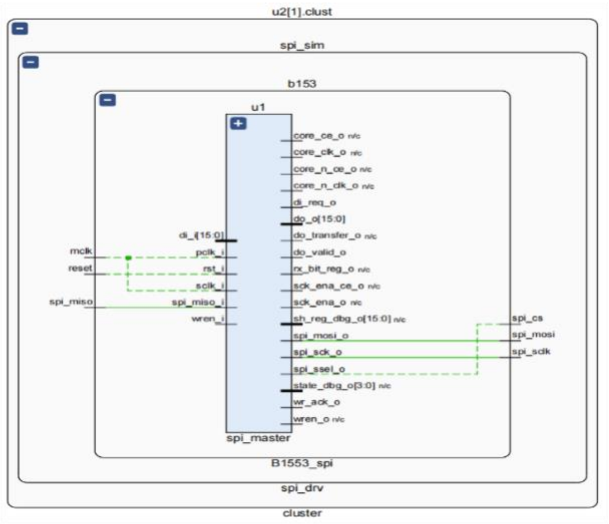

Fig. 7 SPI communication module metafile diagram

Figure 8 shows the initialization module and control module of 1553B. The name of this module is somewhat different from the name of the module interface when it is synthesized, so only the name of the module when it is designed is introduced here. reset indicates the reset signal of the module. mclk, clk_50m and clk_10m indicate the clock signals required by the module, respectively. rt_num Specifies the address of the rt port to be set by the module. sa_idx is the subaddress under the set rt port address. rt_init for 1553B initialization is the enable signal. rt_opcode is the number of steps to initialize and control 1553B. rt_req is the read and write operation request signal during 1553B communication. rt_over indicates the end of RT read and write operations. rt_succ indicates successful initialization of 1553B. rd_reqi is the read operation request signal. wr_reqi is the write request signal. rd_over and wr_over are 1553B, indicating that the read/write operation is complete. wr_word and rd_word are read and write data signals. rd_valid Indicates a valid signal for 1553B read data. data_length Indicates the length of data during read/write operations on module 1553B. start_addr is the start address of 1553B read/write operation, and the interface to communicate with the initial ROM, rt_prom_rden is the read initialization ROM enable signal, rt_prom_addr is the read initialization ROM module address signal, rt_prom_data reads the data signal of the initializing ROM module.

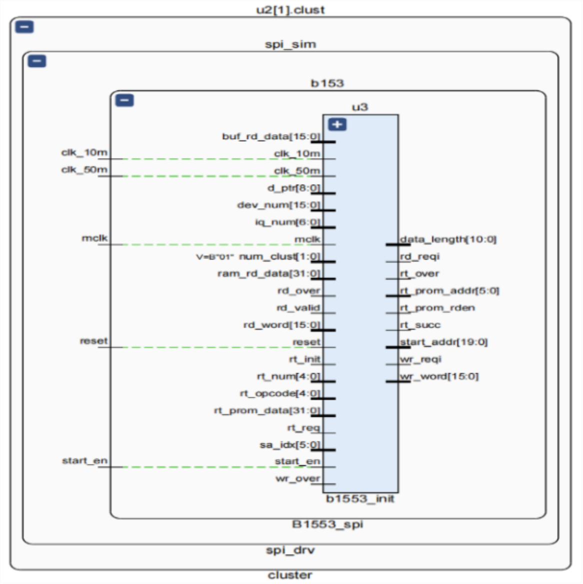

Fig. 8 1553B initialization module metafile diagram

Figure 9 shows the data conversion module, which is responsible for converting 8-bit or 16-bit data read by SPI into 32-bit data, or converting 32-bit data that needs to be sent into the output of the 8-bit or 16-bit SPI module. clk_10m, clk_50m and mclk are clock signals required by the module. data_length Indicates the length of data during the 1553B operation. rd_req and wr_req are read and write request signals. sdata is the data received by SPI. sdata_req is the SPI data request signal. sdata_valid Indicates a valid signal for SPI read data.

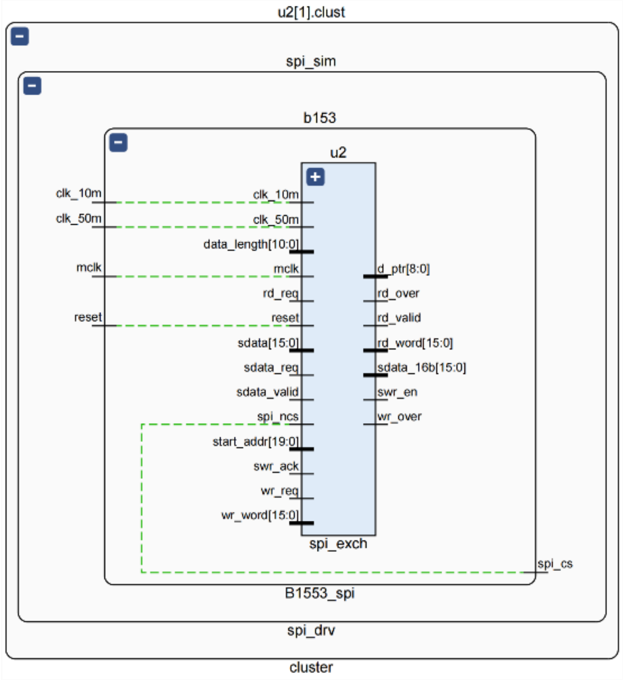

Fig. 9 Data conversion module metafile diagram

4. System test

The communication system of 1553B board card based on FPGA is designed and completed, and the test platform is built in the laboratory, and 1153B configuration and normal communication test is carried out. This communication test was compared with the sequence diagram produced by the MK64F12 version code supplied by the board vendor to verify the results of the 1553B initialization.

Firstly, verify whether RT address enabling operation is carried out normally. Figure 10 shows the RT address enabling sequence diagram of MK64F12 and Figure 11 shows the RT address enabling sequence diagram of FPGA. In order to save resources, some operations are omitted in the FPGA version. As can be seen from the comparison between Figure 10 and Figure 11, the contents of the initial address register are omitted in the FPGA version, and the register is directly configured. And in the contents of the register is RT address 0 x0004 address the configuration of the operation, it is different, the register configuration of contents be: data | rt_addr < < 5 | temp < < 4; Where the data value is 0x0400 and rt_addr is the RT terminal address to be used; temp indicates that the RT terminal address is even. If the RT terminal address is odd, the temp value is 0x0000. Otherwise, the temp is 0x0001. "|" or operation, the "< <" as a left shift operation.

Then verify the configuration of the RT mode start working register. Figure 12 shows the timing diagram of the RT mode start register configured in MK64F12 version, and Figure 13 shows the timing diagram of the RT mode start register configured in FPGA version. By comparing the two figures, it can be seen that the FPGA version successfully configured the RT mode start register.

Figure 14 shows the verification of normal read and write operation of 1553B by FPGA version. It can be seen from the figure that 1553B board controlled by FPGA can carry out normal read and write operation of data.

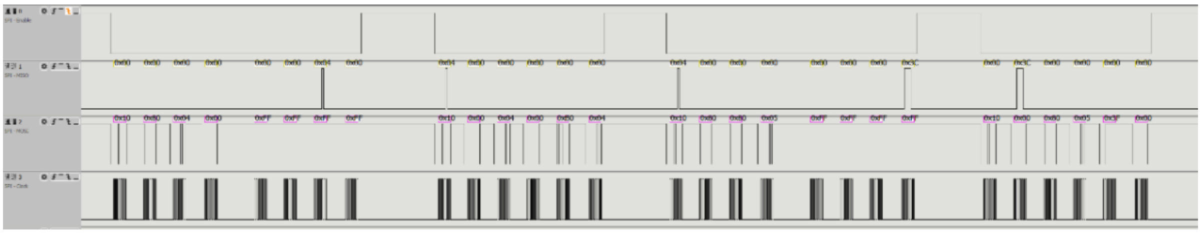

Fig. 10 Sequence diagram of RT address enabling for MK64F12

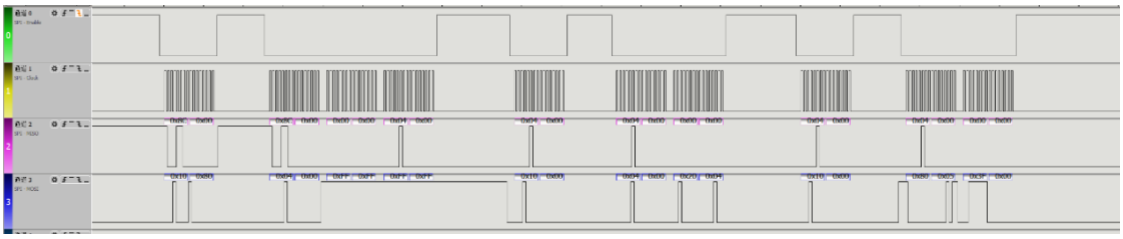

Fig. 11 Timing diagram of RT address enablement in FPGA version

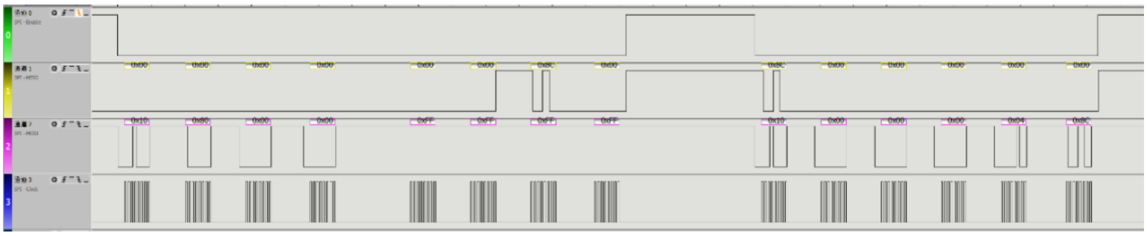

Fig. 12 Timing diagram of RT mode start configuration for MK64F12 version

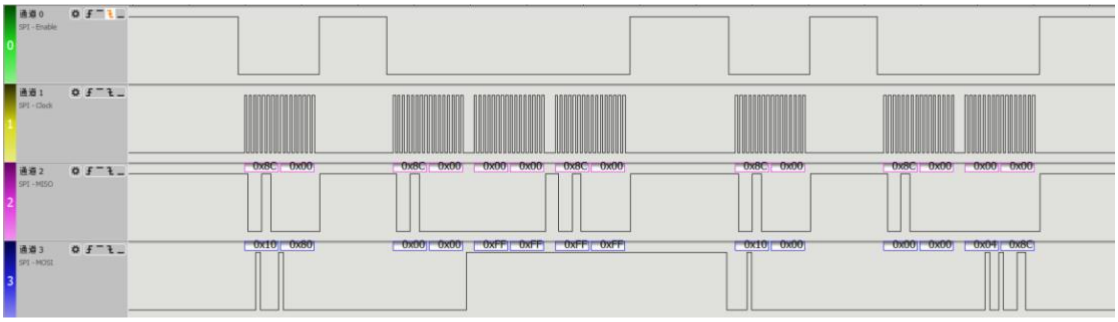

Fig. 13 FPGA version RT mode start configuration timing diagram

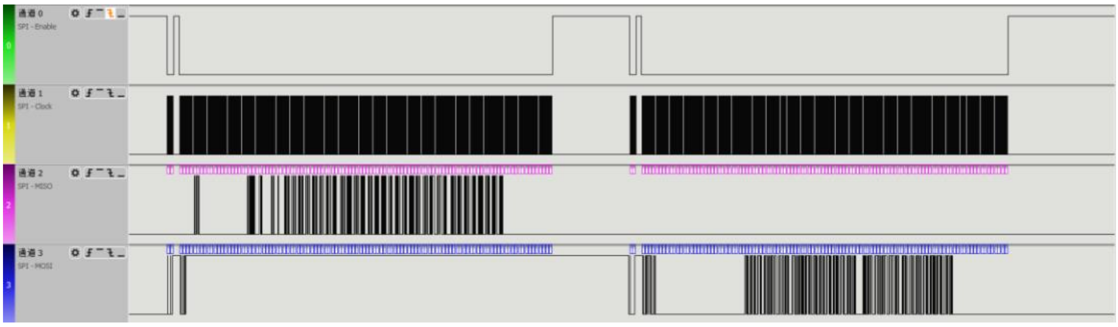

Fig. 14 Sequence diagram of data read and write operation of FPGA version

5. Conclusion

Through the analysis of the waveform collected by the logic analyzer and the further parameter optimization, through the joint test between the board and the commercial 1553B module, it is verified that the 1553B bus communication protocol control system designed based on FPGA is complete and normal, and can run continuously and stably.

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