Journal of Computer Technology and Software

ISSN:2998-2383

Vol. 3, No. 2, 2024

Development of a Compact FPGA-Based ACARS System

Aniruddha Rumale

Gonzaga University

Mdjohar@gmail.com

Abstract: The Aircraft Communication Addressing and Reporting System (ACARS) is a critical component in aircraft communication, facilitating the transmission of identity information between aircraft and ground stations primarily through radio communications. Traditional ACARS systems employ two primary methods for signal processing. The first method involves demodulating the baseband signal using analog techniques followed by decoding with a PC. This approach incurs significant costs, requires multiple frequency conversions which complicate circuit designs and makes debugging challenging. The second method utilizes an Analog-to-Digital Converter (ADC) to sample the analog intermediate frequency (IF) signal, which is then processed digitally. This approach, however, consumes substantial resources in the subsequent processing units, placing considerable strain on the capabilities of the digital signal processors involved.Digital Down Conversion (DDC) is a pivotal technology in communication detection that simplifies this process. DDC shifts the spectrum to reduce or eliminate the carrier frequency of the signal, then utilizes a decimation filter to refine the signal and align it with the requirements of the receiving system. DDC is extensively utilized in software-defined radio and ultra-wideband radar systems.

Keywords: ACARS; ADC; DDC; Signal processing element.

1. Introduction

In 1992, the concept of Software Defined Radio (SDR)was proposed by Jeo Mitola of MITRE Company [1]. It belongs to a new wireless communication architecture. The basic concept is to connect modular and standardized software bus and form a new basic platform, so as to realize the transmission function of wireless communication technology through software loading and open architecture of wireless communication function[2].The application of 5G brings development opportunities to the Internet of Things, and the massive access of the Internet of Things will aggravate the shortage of spectrum resources[3].Today, with the continuous development of information technology, digital down conversion converts the intermediate frequency signal to zero intermediate frequency and reduces the signal rate to a technology suitable for the processing rate of general FPGA devices[4]. Among them, the software provides communication functions, and the hardware device serves as a communication platform, so it does not have to be eliminated with the update of the system. However, the SDR system requires a very high signal sampling rate. Limited by the current hardware level, the back-end hardware device cannot process signals with extremely high rates. At this time, it is necessary to reduce the rate of the initial signal, and digital down converter (DDC) is generated for this purpose. At present, DDC has become an indispensable key technology in software radio, and has gradually become the focus of research. For digital down conversion, dedicated chips and FPGA are very important, so the development of DDC is inseparable from the progress of chips and FPGA. DDC is essentially a mixing method [5]. FPGA is a natural digital signal processor. Its powerful parallel processing ability breaks the sequential execution mode and completes more processing tasks in each clock cycle. At the same time, FPGA can realize the design of combination and timing logic circuits with high precision. [6] It is also a high-speed configurable logic circuit with the characteristics of programmability, flexibility and high integration [7]. Digital down conversion based on FPGA meets the flexible and open requirements of software radio. Considering the problem of performance and cost in FPGA design, combined with the principle of digital down conversion algorithm, the efficient implementation structure of digital down conversion is designed by cascade method according to the characteristics of each stage.

The core of software radio is to make Analog to Digital Converter(ADC) and Digital to Analog Converter(DAC) as close as possible to the RF antenna [8].Based on the open, modular and standard universal platform, most of the functions in the communication system are realized by using software programming with stronger portability, scalability and reusability, and the whole system is liberated from the traditional design ideas based on hardware equipment and functional purposes[9].The common practice is to use digital signal processor[10](Digital Signal Processor, DSP), application specific integrated circuit[11](Application Specific Integrated Circuit, ASIC),field programmable gate array [12](Field Programmable Gate Array, FPGA) and system on a chip[13](System on a Chip, SoC) instead of

special circuits to complete the A / D conversion of the relevant digital signal processing. In this case, the system can be controlled and adjusted by software programming, and the control cost is greatly reduced while the flexibility and versatility are significantly improved. Software radio technology is developed by modern communication technology, microelectronics technology and digital signal processing technology. It has the characteristics of reconfiguration, flexibility, modularization and openness[2], which can transform the traditional system of " single function and poor flexibility " into the structure of " new general standard modeling"[15].The software part of the SDR can be independently updated and upgraded according to the needs of users; the hardware structure can be extended according to the technical indicators[16].At the same time, the compatibility of software radio with the new and old systems reflects its openness, which also ensures the relatively long life cycle of software radio.

Relevant domestic experts and scholars have also made great achievements in the research of receivers in the past decade. Hong Wang et al. from the University of Electronic Science and Technology of China conducted research on digital channelization based on FFT, tree structure and weighted overlap-add(WOLA) structure [17] ; zhang Wen Xu et al. from Harbin Engineering University studied a new efficient structure of digital channelization based on non-maximum extraction of real signals, and also solved the phenomenon of missed alarm and aliasing in channelized receivers[18];huaqiong Li et al.from the Second Institute of Civil Aviation of China proposed a simple, multi-functional digital channelized structure that is easy to implement in hardware.[19];pengfei Tang et al.proposed a digital channelized receiver scheme based on fractional Fourier transform (FRFT) for linear frequency modulation (LFM) signals[20].Chao Lv et al.from Harbin Engineering University deeply studied a new algorithm based on polyphase filtering,and realized a multi-channel receiver based on software radio platform[21].In the"863" plan,"95" and "15" pre-research projects,it is proposed to set SDR technology as the research focus[22].Therefore,the research on software radio system has more far-reaching theoretical significance and more urgent value needs[23].It plays an increasingly wide role in our lives[24-26].

2. Composition principle and analysis

ACARS is an air-ground two-way data communication system. ACARS system is an addressable air / ground communication data transmission system commonly used in international civil aviation at this stage [27]. With the development of civil aviation, civil aviation data link communication is playing an increasingly important role, and the application scope of ACARS is gradually expanding. The automatic transmission of ACARS message reduces the error caused by manual processing and reduces the workload[28].At the same time, the message data transceiver avoids the ambiguity caused by voice communication and improves the real-time performance of the message[29].The ACARS system plays an important role in air traffic control[30], aviation operation control[31],and aviation management control[32].The domestic research based on ACARS system is mainly based on application[33-35].

The ACARS receiving and processing system consists of an analog super-external down-conversion receiver component, a power control unit and a signal processing unit, as shown in Figure 1. Receiver technical indicators are shown in Table 1.

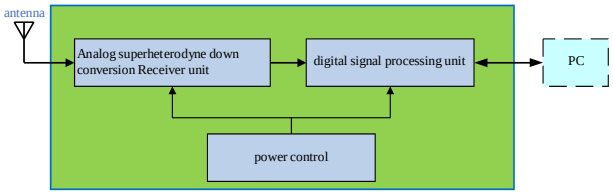

Figure 1. ACARS receiving and processing module block diagram

Table 1. Receiver technical indicators

serial number	technology index		remark
1.	receiving frequency (operating frequency bandwidth)	≥ 118~139 MHz	
2.	receiver 3dB bandwidth	≥ 6 KHz	
3.	dynamic range	≥ 65 dBc	
4.	receiving sensitivity	≤ −100 dBm	
5.	image suppression	≥ 75 dBc	
6.	if rejection ratio	≥ 80 dBc	
7.	third-order cutoff point	≥ +4 dBm	20dB gain test
8.	second-order cutoff point	≥ 40 dBm	
9.	output frequency	70 MHz	
10.	receiver bandwidth	≥ 6 KHz	
11.	output power	0 dBm±2 dB	
12.	AGC response time	≤ 150 ms	
13.	burn-out resistance	Continuous wave 30dBmW	

3. Data Collection by Questionnaire Survey

3.1. Sorting Alternatives Based on Improved TOPSIS

In order to use the orthogonal characteristics of MSK signal 1 code and 0 code waveform to achieve the purpose of reducing the bit error rate, the received MSK signal can be divided into upper and lower branches, and the local carrier frequency of f1 and f2 is used for coherent demodulation to realize the demodulation recovery of the signal. The MSK waveform is shown in Fig.2

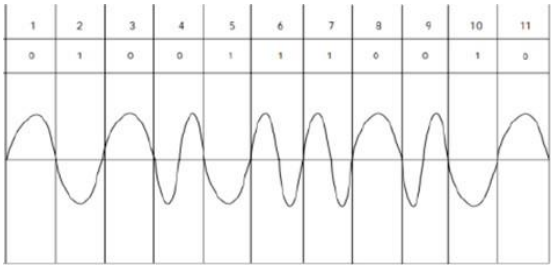

Figure 2. MSK waveform diagram

3.2. MSK demodulation principle block diagram

In Fig.3, the received MSK signal is divided into two branches. The local frequency-shifted carrier cos (2πf1t) and cos (2πf2t) are synchronized with the 1-code and 0-code waveforms of the MSK signal, respectively. Among them, a branch is multiplied and integrated with a carrier frequency of f1 in a cycle, and the result is recorded as P1; another branch is multiplied by the carrier frequency f2 in one cycle, and the result is recorded as P2. Then compare the absolute value of the two, and the frequency is f1 or f2.

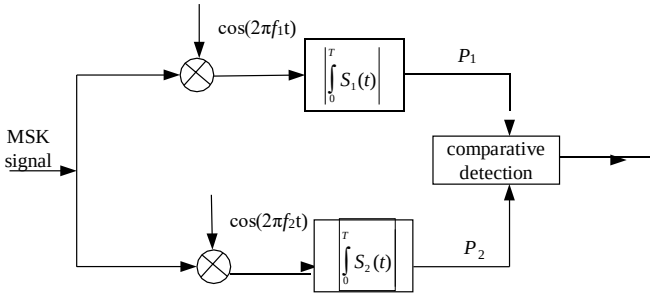

Figure 3. MSK demodulation principle block diagram

4. Conclusion

ACARS (Aircraft Communication Addressing and Reporting System) is one of the avionics communication systems, which is used for digital communication and data transmission between the ground control center and the aircraft in flight. The ACARS system can transmit aircraft performance data, crew information, meteorological information, airport data, etc., which helps to improve the safety and efficiency of air transportation.

The miniaturized ACARS system based on FPGA (Field Programmable Gate Array) is a highly integrated electronic device that integrates multiple modules of the ACARS system (such as modems, data processors, etc.) into one FPGA chip to achieve efficient, stable and reliable data transmission. The system has the advantages of low power consumption, small space occupation and low cost, and is suitable for the application of miniaturized equipment such as aircraft and satellite.

The design of miniaturized ACARS system includes hardware design and software design. The hardware design mainly involves the selection of FPGA chip, the design of system circuit and the design of data interface. The software design mainly involves ACARS protocol analysis, data processing, error detection and correction. At the same time, it is also necessary to consider the real-time, stability and reliability of the system.

In practical applications, the miniaturized ACARS system can be used on the aircraft to realize real-time digital communication and data transmission with the ground control center, which facilitates the decision-making and operation of the crew and improves the safety and efficiency of flight. In addition, the system can also be applied to satellite communication, mobile communication, Internet of things and other fields, with a wide range of application prospects.

In conclusion, the miniaturized ACARS system based on FPGA is highly integrated electronics with wide application prospects.

Acknowledgements

This paper is completed under the careful guidance of teacher Cai. The teacher 's profound professional knowledge, rigorous academic attitude, excellent work style, tireless noble teacher 's ethics, strict self-discipline, generous treatment of people 's lofty style, simple and unadorned, approachable personality charm have a profound impact on me. It is not only that I have set up ambitious academic goals and mastered basic research methods, but also that I have understood many ways to deal with people.

I would also like to thank my family, teachers and my classmates and friends who gave me great concern and support during my postgraduate study. This design can be successfully completed, but also thanks to the teachers ' serious and responsible, so that I can grasp and use professional knowledge, and can be reflected in the design. It is your constant support, help and meticulous care in life and study. It is you who constantly give me confidence and let me go strong again and again in life. It is with their careful help and support that my graduation thesis work is successfully completed. Once again, I express my heartfelt thanks to all teachers for their unknown hard cultivation. (School of Automation and Information Engineering, Sichuan University of Science & Engineering).

Fund project: Vibration displacement measurement of robot servo system based on machine vision, Fund number: Y2022128.

References

[1] MITOLA J. The software radio architecture[J/OL]. IEEE Communications Magazine, 1995, 33(5): 26-38. DOI:10.1109/35.393001.

[2] Xu Wenbin. Application research of software radio technology in 5G mobile communication system [J]. China New Communications, 2020, 22 (11) : 22.

[3] Dai.Research and implementation of software radio digital spectrum analysis technology based on SOPC [D].University of Electronic Science and Technology of China, 2019.

[4] Chen, Qu, Li et al. [4].A processing method and implementation of radar digital IF receiver [J / OL].Journal of Radio Wave Science, 2014,29 (06) : 1212-1218. [5][]Yin

[5] Zhaoyun. Design of software radio digital down conversion technology based on FPGA [D]. Guangdong University of Technology, 2015.

[6] Wang Wei.Development of FPGA in the era of Internet of Things [J].Electronic technology application, 2017,43 (02) : 9.

[7] Zhou Xiaole. Design and implementation of digital down conversion [D]. Xidian University, 2015.

[8] Niu Wei.Application of Software Radio Technology in the Field of Mobile Communication Testing [J / OL].Electronic World, 2018 (11) : 169-170.

[9] Research and FPGA implementation of wireless receiver channel digitization [D].University of Electronic Science and Technology of China, 2018.

[10] Zhou Honghang.Research on digital signal processing technology in single-carrier high-speed optical communication system [D].Beijing University of Posts and Telecommunications, 2021.

[11] Zhao Boya.Research on the design and implementation of hardware accelerator based on convolutional neural network [D].Harbin University of Technology, 2018.

[12] Cao Xueyao.Research and design of Beidou positioning terminal based on FPGA [D].Changchun University of Technology, 2022.

[13] Zhang Siyun.Design of H.264 decoding SOC for real-time video transmission system [D].Jilin University, 2020.

[14] Zhang Xuecheng.Analyze the application of software radio technology in modern communication system [J].Wireless interconnection technology, 2014 (01) : 74.

[15] Liu Jian. Design and implementation of AIS & ACARS IF digital receiver [D]. Harbin Engineering University, 2013.

[16] Li Mu.Research on ACARS signal receiving technology based on software radio technology [D].Harbin University of Technology, 2015.

[17] HAIFENG WANG, LU Y. A digital channelized receiver architecture with low calculation cost[C/OL]//2010 Second Pacific-Asia Conference on Circuits, Communications and System. Beijing, China: IEEE, 2010: 1-4. DOI: 10.1109/ PACCS. 2010.5627076.

[18] XU Z W, MING S F, TONG L, et al. Model of Non-leaking-Alarms and Non-aliasing Channelized Digital Receiver [C/OL] // 2016 Sixth International Conference on Instrumentation & Measurement, Computer, Communication and Control (IMCCC). Harbin, China: IEEE, 2016: 994-997. DOI: 10.1109 / IMCCC.2016.53.

[19] XU S. Design and Implementation of Digital Channelized Receiver in Multi-FPGA[C/OL]//2009 First International Conference on Information Science and Engineering. Nanjing, China: IEEE, 2009: 178-181. DOI:10.1109/ICISE.2009.461.

[20] TANG P, YUAN B, BAO Q, et al. Design and simulation of digital channelized receivers in fractional Fourier domain[J/OL]. Journal of Systems Engineering and Electronics, 2013, 24(1): 36-43. DOI:10.1109/JSEE.2013.00005.

[21] LV C, LIN Y. One kind of channelized receiver structure applied to software radio platform[C/OL]//Proceedings of 2014 3rd Asia-Pacific Conference on Antennas and Propagation. Harbin, China: IEEE, 2014: 810-813. DOI: 10.1109 / APCAP.2014.6992622.

[22] Li Cheng, Lu Yanfei, Lai Wei, et al. Design and practice of remote software radio open experimental platform [J / OL]. Experimental technology and management, 2018,35 (02) : 103-107. DOI: 10.16791 / j.cnki.sjg.2018.02.025.

[23] Wang Yan. Simulation study of digital IF chip [J]. Communication technology, 2020 (03 vo 53) : 776-780.

[24] Peng Feng.Technical characteristics and application of software radio [J / OL].Electronic test, 2021 (06) : 71-72 + 126.DOI : 10.16520 / j.cnki.1000-8519.2021.06.03.

[25] HALDORAI A, KANDASWAMY U. Software Radio Architecture: A Mathematical Perspective [M/OL] // HALDORAI A, KANDASWAMY U. Intelligent Spectrum Handovers in Cognitive Radio Networks. Cham: Springer International Publishing, 2019: 65-86. DOI: 10.1007 / 978-3-030-15416-5_4.

[26] GAO J. Analysis of Military Application of Software Radio Communication Technology[J/OL]. MATEC Web of Conferences, 2019, 267: 02017. DOI: 10.1051 / matecconf / 201926702017.

[27] RAZA A, ULANSKY V. Through-Life Maintenance Cost of Digital Avionics[J/OL]. Applied Sciences, 2021, 11(2): 715. DOI:10.3390/app11020715.

[28] Wang Minjie, Wen Ronghui, Chen Yujun. Research on anti-interference performance of MSK demodulation method based on ACARS data link [J / OL].Modern Information Technology, 2020,4 (06) : 61-64 + 68. DOI: 10.19850 / j.cnki.2096-4706.2020.06.021.

[29] SMITH M, MOSER D, STROHMEIER M, et al. Undermining Privacy in the Aircraft Communications Addressing and Reporting System (ACARS)[J/OL]. Proceedings on Privacy Enhancing Technologies, 2018, 2018(3): 105-122. DOI:10.1515/popets-2018-0023.

[30] KITAORI J. A performance comparison between VDL mode 2 and VHF ACARS by protocol simulator[C/OL]//2009 IEEE/AIAA 28th Digital Avionics Systems Conference. Orlando, FL, USA: IEEE, 2009: 4.B.3-1-4.B.3-8. DOI:10.1109/DASC.2009.5347498.

[31] SMITH M, MOSER D, STROHMEIER M, et al. Economy Class Crypto: Exploring Weak Cipher Usage in Avionic Communications via ACARS[M/OL]//KIAYIAS A. Financial Cryptography and Data Security: Vol. 10322. Cham: Springer International Publishing, 2017: 285-301. DOI:10.1007/978-3-319-70972-7_15.

[32] HAN P, HUI H, LU X, et al. A Research and Implementation on Real Time Tracking for Abnormal Flight using ACARS[C/OL]//2018 IEEE/AIAA 37th Digital Avionics Systems Conference (DASC). London: IEEE, 2018: 1-6. DOI:10.1109/DASC.2018.8569830.

[33] Zhao Jun, Tang Yidi.Research on civil aviation engine condition monitoring based on ACARS data [J].Computer simulation, 2020, 37(08): 49-52.

[34] LIN L, LIU J, GUO H, et al. Sample adaptive aero-engine gas-path performance prognostic model modeling method[J/OL]. Knowledge-Based Systems, 2021, 224: 107072. DOI: 10.1016 / j.knosys.2021.107072.

[35] XU H, XIAO K, PAN J, et al. Evidence of aircraft activity impact on local air quality: A study in the context of uncommon airport operation[J/OL]. Journal of Environmental Sciences, 2023, 125: 603-615. DOI: 10.1016 / j.jes.2022.02.039.