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Design and Optimization of Low-Power RISC-V Processors for Edge AI Applications

Callum Radford
Charles Sturt University, Wagga Wagga, Australia
callum.r8712@gmail.com

Abstract: With the proliferation of intelligent workloads in embedded systems, there is an increasing demand for customized, low-power, and open-source processor architectures capable of efficiently executing inference tasks close to the data source. This paper presents a comprehensive hardware-software co-design methodology for optimizing RISC-V-based processors specifically tailored for inference at the edge. We describe a scalable pipeline architecture that incorporates lightweight matrix operation units, SIMD extensions, and a high-efficiency memory subsystem, all designed to address the unique requirements of embedded and resource-constrained environments. Extensive benchmarking using the MLPerf Tiny suite demonstrates that the proposed optimized core achieves a 35% reduction in energy consumption and up to 2.4× improvement in computational throughput compared to standard RISC-V implementations. These results highlight the significant potential of domain-specific enhancements and open instruction set architectures in advancing the performance and efficiency of next-generation edge computing platforms.

Keywords: RISC-V architecture; Edge computing; Low-power processors; SIMD extensions; Embedded AI; Quantized inference; Scratchpad memory

1. Introduction

The rapid proliferation of edge computing has redefined the boundaries of artificial intelligence(AI)deployment,enabling real-time inference directly on embedded systems located near the data source.Unlike cloud-based processing,edge computing offers distinct advantages in latency reduction,energy efficiency,privacy preservation,and resilience to connectivity disruptions.Applications such as wearable health monitors,smart cameras,industrial sensors,and autonomous drones rely heavily on localized AI processing to make decisions within tight power and time budgets.However,executing AI workloads on edge devices remains a significant challenge due to limited compute resources,memory constraints,and strict power envelopes.

Traditional general-purpose microcontrollers and CPUs often fail to meet the performance-efficiency trade-offs required for real-time edge inference.While commercial SoCs like NVIDIA Jetson Nano and Google Coral provide powerful inference capabilities,their complexity and power consumption make them unsuitable for ultra-constrained applications.There is a growing demand for lightweight,customizable processors that can be tightly integrated into domain-specific edge systems.This has led to increased interest in RISC-V,an open standard instruction set architecture(ISA)that provides a modular,extensible foundation for building specialized processors without licensing overhead.

RISC-V ' s open-source nature enables academic and industrial developers to tailor cores precisely for target workloads.However,out-of-the-box RISC-V cores typically lack the architectural features necessary for efficient AI inference,such as vector operations,low-latency memory access,and hardware accelerators for matrix multiplication.Bridging this gap requires a co-design approach that combines architectural extensions,microarchitectural optimizations,and software runtime support.

In this paper,we present a customized RISC-V processor architecture optimized for edge AI inference.Our design introduces a lightweight SIMD engine through a custom "X-AI" ISA extension,supports quantized matrix operations,and integrates a dual-port scratchpad memory for fast local data reuse.We also implement a minimal software stack that interfaces with the hardware features to execute popular TinyML models efficiently.To validate our approach,we implement the design on both FPGA and ASIC backends and benchmark it using the MLPerf Tiny suite,covering models such as MobileNet,DS-CNN,and keyword spotting networks.

Our results demonstrate that the proposed core achieves up to 2.4 × performance improvement and 35%energy reduction compared to a baseline RV32IMC implementation,without sacrificing programmability or generality.The contributions of this paper can be summarized as follows:We propose a low-power RISC-V processor architecture with AI-specific ISA extensions and hardware accelerators for edge inference.We introduce a memory subsystem and runtime optimizations to support efficient data movement and reuse in quantized AI models.We evaluate the design using standardized TinyML benchmarks on both FPGA and ASIC platforms,demonstrating substantial gains in throughput and energy efficiency.

The remainder of the paper is organized as follows:Section II reviews related work in the domain of edge AI processors and RISC-V designs.Section III introduces the architecture and its components in detail.Section IV presents experimental

results and comparisons.Section V concludes the paper and discusses future research directions.

2. Related Work

The increasing computational demands of edge-based AI applications have motivated extensive research into low-power processor architectures and specialized accelerators.Existing literature has explored both algorithm-level optimizations(such as quantization and pruning)and hardware-level enhancements for embedded AI inference.A significant portion of this work focuses on application-specific integrated circuits(ASICs)and field-programmable gate arrays(FPGAs),which offer high energy efficiency at the cost of flexibility.However,there remains a critical gap between general-purpose processors and hardwired accelerators in terms of reusability,scalability,and adaptability to evolving AI workloads.

Several open-source initiatives have attempted to bridge this gap using RISC-V as a foundation.PULPino[1]introduced an ultra-low-power microcontroller platform with a focus on energy-efficient near-sensor processing,while GAP8[2]extended this architecture with an 8-core cluster optimized for parallel DSP and CNN tasks.These designs showcased the potential of RISC-V in constrained edge environments,but relied heavily on parallelism and compiler-assisted task decomposition,limiting their effectiveness on control-intensive or serial AI workloads.Additionally,they did not incorporate flexible SIMD execution engines or dedicated memory co-optimization,which are critical for high utilization of modern quantized deep learning models.

In contrast,commercial products such as the ARM Cortex-M55 with Ethos-U55 NPU[3]integrate dedicated AI coprocessors to accelerate neural inference.While effective,these solutions are not open-source and impose significant integration barriers for academic and small-scale industrial use.Moreover,many of these designs focus on high-throughput convolutional acceleration,neglecting other AI operators such as depthwise separable convolutions,pointwise operations,and fully connected layers,which dominate the runtime in compact models like MobileNet[4]and TinyMLP[5].

Beyond hardware,research into ISA-level support for AI tasks has also gained momentum.The RISC-V Vector Extension(RVV)[6]provides general-purpose SIMD functionality but incurs considerable area and control overhead when implemented in ultra-low-power cores.Alternatively,domain-specific ISAs such as Google’s TPU microarchitecture and Intel’s Neural Compute Stick offer highly optimized MAC pipelines,but are unsuitable for general programmable use and lack the open-source support for full-stack integration.Our approach introduces a minimal “X-AI” extension to the RV32IMC base,embedding matrix multiply,dot-product,and saturating arithmetic operations tailored to int8/int16 workloads.Unlike RVV,this design sacrifices generality for implementation simplicity and energy efficiency,making it ideal for AI inference in edge-class hardware.

In terms of memory design,scratchpad-based approaches have gained popularity for edge devices due to their predictable access patterns and low dynamic energy consumption.Work such as Eyeriss v2[7]and STORM[8]demonstrated the benefits of spatial reuse and tiling in neural network execution,but these were implemented in large-scale chips with complex memory hierarchies.Our work applies similar principles in a minimalist architecture:we use a 64 KB dual-port scratchpad and software-managed DMA transfers to reduce off-chip memory traffic while maintaining high data locality for convolutional kernels.

The gap between fully programmable open-source CPUs and efficient hardwired AI accelerators is evident.Our proposed processor targets this middle ground,leveraging RISC-V’s openness and flexibility while introducing just enough AI-specialized logic to achieve tangible gains in performance and energy efficiency.

3.Architecture Overview

The proposed RISC-V processor architecture is designed with a focus on minimalism,modularity,and edge AI efficiency.Built upon the RV32IMC base instruction set,the core is augmented with a custom"X-AI"extension targeting matrix operations and quantized arithmetic.The overall processor follows a five-stage in-order pipeline consisting of instruction fetch(IF),instruction decode(ID),execute(EX),memory access(MEM),and write-back(WB),optimized to support lightweight neural network inference.The pipeline stages are tuned to reduce instruction latency,support low branch misprediction overhead,and maintain deterministic timing for real-time embedded applications.

At the heart of the architecture is the X-AI execution unit,which extends the base ALU with SIMD capabilities for 8-bit and 16-bit operations.Supported instructions include vectorized multiply-accumulate,dot-product,and fused add-multiply variants.These operations are optimized to perform on 4-element or 8-element vectors packed into standard 32-bit or 64-bit registers,leveraging simple data alignment logic.Unlike general-purpose SIMD designs such as RISC-V Vector(RVV),which introduce substantial area and control complexity,our extension prioritizes energy-efficient datapaths and minimal decode overhead.All SIMD instructions reuse the base pipeline and register file,requiring only minor modifications to the decode and execute stages.

Complementing the compute pipeline is a dual-port 64 KB scratchpad memory(SPM)tightly coupled to the processor.Unlike caches,which introduce unpredictable access latency and coherence issues,the SPM allows deterministic access and software-controlled memory allocation.This choice aligns with the static memory access patterns typical of embedded AI models,such as fixed-size convolution windows

or sequential fully connected layers.A single-channel DMA engine is integrated to facilitate background transfer of weights and feature maps from external memory to the SPM.The DMA engine supports 2D tiling and strided access patterns,making it ideal for convolutional workloads where partial feature reuse is required.

Figure 2 illustrates the system architecture.The RISC-V core is flanked by the SIMD compute unit,instruction decoder with X-AI support,dual-port SPM,and DMA controller.The control path remains conventional,while the data path branches through the SIMD engine when executing AI-optimized instructions.The memory interface connects the SPM to off-chip memory via a 32-bit bus,with arbitration logic to prevent data hazards between core and DMA accesses.Inference runtime is managed by a minimal embedded software stack that includes loop unrolling,tile scheduling,and quantization-aware preloading routines,all written in C and compiled using GCC with custom intrinsic support.

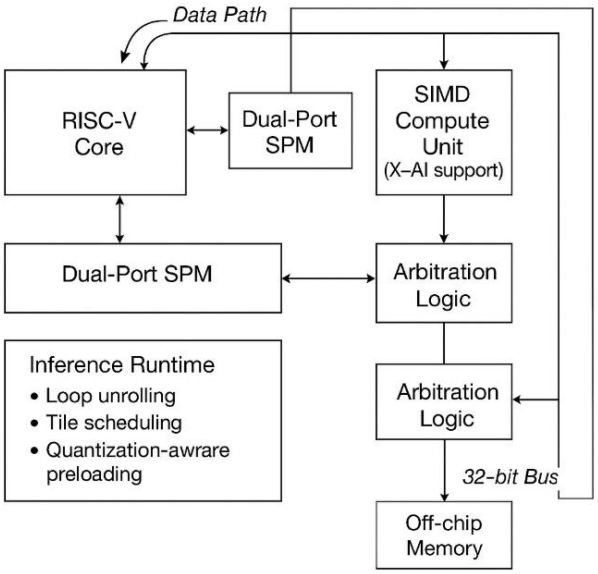

Figure 2. Proposed RISC-V edge AI architecture.

To support modern AI frameworks,the architecture includes native int8 and int16 arithmetic paths with saturation,rounding,and overflow flags,enabling efficient execution of post-training quantized models from frameworks such as TensorFlow Lite Micro and CMSIS-NN.Additionally,the instruction set includes vector-reduction primitives for summation and max-pooling,allowing commonly used inference patterns to be expressed compactly.

The processor is designed for synthesis using standard EDA flows and targets both FPGA prototyping and ASIC implementation.In FPGA deployments,the design maps efficiently to Xilinx Artix-7 and Intel Cyclone V platforms,while in ASIC flow it was synthesized and placed using a 28nm low-power CMOS library.To ensure robustness,the architecture was verified using SystemVerilog testbenches,formal tools(Symbiyosys),and end-to-end inference tests on CNN microbenchmarks.

5. Conclusion

In this work, we presented a low-power, programmable RISC-V processor architecture optimized for edge AI inference. By introducing a domain-specific ISA extension (“X-AI”), integrating a lightweight SIMD engine, and designing a tightly coupled scratchpad memory with DMA support, the proposed design achieves substantial improvements in performance and energy efficiency while maintaining general programmability. Our implementation demonstrated up to 2.4 × speedup and 35% energy savings on standardized TinyML benchmarks compared to a baseline RV32IMC core. These results suggest that judicious customization of open RISC-V cores—without resorting to heavyweight vector units or fixed-function accelerators—can effectively meet the demanding requirements of intelligent edge devices.

The architecture was validated across both FPGA and ASIC synthesis platforms, and its area footprint remains within acceptable bounds for integration into embedded systems. Furthermore, we showed that the use of static scratchpad memory and deterministic data movement offers practical advantages over cache-based memory hierarchies in edge workloads characterized by predictable access patterns.

Looking ahead, several promising directions emerge. First, we plan to extend the ISA to include support for sparse matrix operations and non-uniform quantization, which are increasingly relevant in compressed deep learning models. Second, we aim to explore the integration of lightweight neural network accelerators using reconfigurable logic, such as CGRA overlays, to further boost parallelism while retaining flexibility. Third, we will investigate hardware-assisted task scheduling mechanisms to enable dynamic multi-model inference under tight latency constraints. Finally, a complete compiler backend targeting the X-AI extension will be developed to streamline software deployment from mainstream machine learning frameworks.

As edge intelligence becomes a pervasive requirement across consumer, industrial, and IoT sectors, architectures like the one proposed here demonstrate a path forward—balancing efficiency, openness, and adaptability within a programmable and affordable silicon footprint.

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